***§112 Rejection of the Claims***

Claims 11-25 and 35-43 were rejected under 35 USC § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention.

The language "layer of scribe material" has been removed from all pending claims. The removal of the language from the claims was not related to the pending § 112 rejection. Therefore, the relevant claim amendments should not be construed as an acknowledgement that the rejection was appropriate. Applicant notes that the language is supported by Applicant's specification at page 1, lines 21-26; page 5 line 29 through page 6, line 3; page 6, line 28 through page 7, line 5; and Figures 2 and 3.

The Office Action also alleges that the terms "ground" and "polished" are indefinite. Applicant respectfully disagrees regarding the indefiniteness of the terms. The Board of Patent Appeals and Interferences has stated:

> In rejecting a claim under the second paragraph of 35 U.S.C.§112, it is incumbent on the examiner to establish that one of ordinary skill in the pertinent art, when reading the claims in light of the supporting specification, would not have been able to ascertain with a reasonable degree of precision and particularity the particular area set out and circumscribed by the claims. *Ex parte* Wu, 10 USPQ 2d 2031, 2033 (B.P.A.I. 1989)(citing *In re* Moore, 439 F.2d 1232, 169 USPQ 236 (C.C.P.A. 1971); *In re* Hammack, 427 F.2d 1378, 166 USPQ 204 (C.C.P.A. 1970)).

The M.P.E.P. adopts this line of reasoning, stating that:

> The essential inquiry pertaining to this requirement is whether the claims set out and circumscribe a particular subject matter with a reasonable degree of clarity and particularity. Definiteness of claim language must be analyzed, not in a vacuum, but in light of:
>
> (1) The content of the particular application disclosure;
> (2) The teachings of the prior art; and
> (3) The claim interpretation that would be given by one possessing the ordinary level of skill in the pertinent art at the time the invention was made. *M.P.E.P.* § 2173.02.

Applicant respectfully submits that the claim language in question, when analyzed in light of the content of the application disclosure, is not indefinite. The application disclosure discusses grinding or polishing a cut edge at page 2, lines 16-28. The application disclosure further describes grinding or polishing at page 5, lines 8-14 and compares a cut edge versus a

ground or polished edge at page 5, lines 15-18 and FIGS. 2 and 3. In addition, at page 6, line 6 through page 7, line 5, the specification describes the problems associated with cut edges versus ground edges such that one of ordinary skill in the art could recognize a cut edge versus a ground or polished edge.

Reconsideration and allowance of claims 11-25, 36-39 and 41-43 is respectfully requested.

***§102 Rejection of the Claims***

Claims 11-25 and 35-43 were rejected under 35 USC § 102(b) as being anticipated by Ormond et al. (U.S. Patent No. 5,128,282). "For a prior art reference to anticipate in terms of 35 U.S.C. § 102, every element of the claimed invention must be identically shown in a single reference." (emphasis added). *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566, 1567 (Fed. Cir. 1990). "The identical invention must be shown in as complete detail as is contained in the . . . claim." *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

*Claims 11-14*

Applicant cannot find in Ormond "one or more planar perimeter side surfaces, each planar perimeter side surface extending from the first planar surface to the second planar surface" in combination with "each planar perimeter side surface of the semiconductor die being a ground or polished surface" as recited in claim 11. As discussed during the interview, applicant respectfully directs the Examiner's attention to wall 35 in FIGS. 3-5 of Ormond.

Claims 12-14 depend from claim 11 such that they incorporate all of the limitations of claim 11. Therefore, Applicant respectfully requests allowance of claims 12-14 for the reasons provided above with regard to claim 11.

Reconsideration and allowance of claims 11-14 is respectfully requested.

*Claim 15-17*

Applicant again directs the Examiner's attention to wall 35 in FIGS. 3-5 of Ormond. Applicant cannot find in Ormond "one or more planar perimeter side surfaces, at least one of the planar perimeter side surfaces extending from the first planar surface to the second planar

surface, the entire at least one perimeter side surface having a ground or polished surface" as recited in claim 15.

Claims 16-17 depend from claim 15 such that they incorporate all of the limitations of claim 15. Therefore, Applicant respectfully requests allowance of claims 16-17 for the reasons provided above with regard to claim 15.

Reconsideration and allowance of claims 15-17 is respectfully requested.

*Claims 18-21*

Applicant cannot find in Ormond "at least one perimeter side surface having at least two offset planar surfaces, where the at least two offset planar surfaces are substantially parallel to each other and ground or polished" as recited in claim 18.

Claims 19-21 depend from claim 18 such that they incorporate all of the limitations of claim 18. Therefore, Applicant respectfully requests allowance of claims 18-21 for the reasons provided above with regard to claim 18.

Applicant notes that end 11 of Ormond appears to be a surface exposed by dicing blade 60. FIG. 5 of Ormond shows that only a portion of the die's side surface is formed by groove 40 because the dicing blade 60 cuts through tab 15 to form die 5 (see col. 6, lines 27-28). Therefore, the entire side surface appears to formed by edge 11, groove 40 and wall 35 with edge 11 including a surface exposed by cutting instead of a ground or polished surface.

It is unclear how Ormond teaches, among other things, at least one perimeter side surface having at least two offset planar surfaces, where the at least two offset planar surfaces are substantially parallel to each other and ground or polished as recited in claim 18. By failing to teach such structure, Ormond does not meet the standard set forth in *In re Bond* requiring that "every element of the claimed invention must be identically shown in a single reference." 910 F.2d at 831, 15 USPQ2d at 1566, 1567.

As discussed during the interview, Applicant respectfully submits that a polished or ground surface is not the same as a surface exposed by cutting, such as end 11 of Ormond. The specification in Ormond recognizes this at col. 1, lines 46-61, col. 2, lines 10-21 and col. 5, lines 6-22. Applicant also refers the Examiner to Applicant's own specification at page 6, lines 6-19, which recognizes the problems associated with die edges formed by cutting.

Reconsideration and allowance of claims 18-21 is respectfully requested.

*Claims 22-24*

Applicant incorporates the above discussion of Ormond herein. Applicant cannot find in Ormond "at least one of the perimeter sides having at least two offset planar surfaces that are substantially parallel to each other and ground or polished to remove irregularities from each of the two offset planar surfaces" as recited in claim 22.

Claims 23 and 24 depend from claim 22 such that they incorporate all of the limitations of claim 22. Therefore, Applicant respectfully requests allowance of claim 22-24 for the reasons provided above with regard to claim 22.

Reconsideration and allowance of claims 22-24 is respectfully requested.

*Claim 25*

Applicant incorporates the above discussion of Ormond herein and again refers to wall 35 in FIGS. 3-5 of Ormond. Applicant cannot find in Ormond "each perimeter side having offset perimeter planar surfaces, where the offset perimeter planar surfaces are substantially parallel to each other with one of the offset perimeter planar surfaces extending from the first planar surface and another of the offset perimeter planar surfaces extending from the second planar surface, and each of the offset perimeter planar surfaces is a ground or polished surface" as recited in claim 25. As discussed during the interview, applicant respectfully directs the Examiner's attention to wall 35 in the FIGS. of Ormond.

Reconsideration and allowance of claim 25 is respectfully requested.

*Claims 35-39*

Applicant incorporates the above discussion of Ormond herein. Applicant cannot find in Ormond "at least one perimeter side having two or more offset planar perimeter surfaces, each of the two or more offset planar perimeter surfaces being ground or polished surfaces with one of the offset perimeter planar surfaces extending from the first planar surface and another of the offset perimeter planar surfaces extending from the second planar surface" as recited in claim 35.

As discussed during the interview, applicant respectfully directs the Examiner's attention to walls 35, 36 in the FIGS. of Ormond.

Claims 36-39 depend from claim 35 such that they incorporate all of the limitations of claim 35. Therefore, Applicant respectfully requests reconsideration and allowance of claims 35-39 for the reasons provided above with regard to claim 35.

*Claims 41-43*

Applicant incorporates the above discussion of Ormond herein. Applicant cannot find in Ormond "at least one perimeter edge having two or more offset planar surfaces, where the offset planar surfaces are substantially transverse to the first planar surface or the second planar surface with one of the offset planar surfaces extending from the first planar surface and the other of the offset planar surfaces extending from the second planar surface" as recited in claim 41.

As discussed above, it is unclear how Ormond teaches, among other things, that each offset planar surface is ground or polished when edge 11 in Ormond is exposed by cutting. By failing to teach such structure, Ormond does not meet the standard set forth in *In re Bond* requiring that "every element of the claimed invention must be identically shown in a single reference." 910 F.2d at 831, 15 USPQ2d at 1566, 1567.

Claims 42-43 depend from claim 41 such that they incorporate all of the limitations of claim 41. Therefore, Applicant respectfully requests reconsideration and allowance of claims 41-43 for the reasons provided above with regard to claim 41.

*Conclusion*

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 359-3276 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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Date Jan 17, 2003

By _____
Catherine I. Klima-Silberg
Reg. No. 40,052

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 17th day of January, 2003.

Amy Moriarty
Name

_____
Signature

Docket No. 303.259US3
*WD # 402391*

Micron Ref. No. 96-0587.02

**CLEAN VERSION OF PENDING CLAIMS**

GRINDING TECHNIQUE FOR INTEGRATED CIRCUITS
Applicant: Aaron M. Schoenfeld
Serial No.: 09/785,006

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*Claims 11-25, 35-39, and 41-43, as of January 18, 2003 (Date of Response to First Office Action after RCE filed).*

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11. (Twice Amended) A semiconductor die comprising:

a first planar surface having circuitry thereon;

a second planar surface opposite the first planar surface;

one or more planar perimeter side surfaces, each planar perimeter side surface extending from the first planar surface to the second planar surface;

and

each planar perimeter side surface of the semiconductor die being a ground or polished surface.

G1

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12. The semiconductor die as recited in claim 11, wherein each planar perimeter side surface is transverse to the first planar surface and the second planar surface.

13. The semiconductor die as recited in claim 11, wherein the semiconductor die has a substantially rectangular shape.

14. The semiconductor die as recited in claim 11, wherein each planar perimeter surface is a ground surface.

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15. (Twice Amended) A semiconductor die comprising:

a first planar surface having circuitry thereon;

a second planar surface opposite the first planar surface;

G2 cont'd

G2 end

one or more planar perimeter side surfaces, at least one of the planar perimeter side surfaces extending from the first planar surface to the second planar surface, the entire at least one perimeter side surface having a ground or polished surface.

16. The semiconductor die as recited in claim 15, wherein each planar perimeter side surface is transverse to the first planar surface and the second planar surface.

17. The semiconductor die as recited in claim 15, wherein each planar perimeter side surface comprises a polished surface.

18. A semiconductor die comprising:

a first planar surface having circuitry thereon;

a second planar surface opposite the first planar surface;

one or more perimeter side surfaces extending between the first planar surface and the second planar surface; and

at least one perimeter side surface having at least two offset planar surfaces, where the at least two offset planar surfaces are substantially parallel to each other and ground or polished.

19. The semiconductor die as recited in claim 18, wherein the semiconductor die comprises a rectangular die.

20. The semiconductor die as recited in claim 18, wherein each perimeter side surface has offset planar surfaces.

21. The semiconductor die as recited in claim 18, wherein the at least two offset planar surfaces are transverse to the first planar surface and the second planar surface.

22. (Twice Amended) A semiconductor die comprising:

a first planar surface having circuitry thereon;

a second planar surface opposite the first planar surface;

one or more perimeter sides;

and

at least one of the perimeter sides having at least two offset planar surfaces that are substantially parallel to each other and ground or polished to remove irregularities from each of the two offset planar surfaces.

G3

23. (Twice Amended) The semiconductor die as recited in claim 22, wherein each of the two offset planar surfaces is transverse to the first planar surface and the second planar surface.

24. (Twice Amended) The semiconductor die as recited in claim 22, wherein at least one of the two offset planar surfaces extends from at least one of the first planar surface and the second planar surface.

25. (Twice Amended) A semiconductor die comprising:

a first planar surface having circuitry thereon;

a second planar surface opposite the first planar surface;

one or more perimeter sides extending between the first planar surface and the second planar surface;

each perimeter side having offset perimeter planar surfaces, where the offset perimeter planar surfaces are substantially parallel to each other with one of the offset perimeter planar surfaces extending from the first planar surface and another of the offset perimeter planar surfaces extending from the second planar surface, and each of the offset perimeter planar surfaces is a ground or polished surface.

35. (Twice Amended) A semiconductor die comprising:

a first planar surface having circuitry thereon;

a second planar surface opposite the first planar surface;

G4

one or more perimeter sides extending between the first planar surface and the second planar surface; and

at least one perimeter side having two or more offset planar perimeter surfaces, each of the two or more offset planar perimeter surfaces being ground or polished surfaces with one of the offset perimeter planar surfaces extending from the first planar surface and another of the offset perimeter planar surfaces extending from the second planar surface.

36. The semiconductor die as recited in claim 35, wherein each of the two or more offset planar perimeter surfaces is transverse to the first planar surface and the second planar surface .

37. The semiconductor die as recited in claim 35, wherein the semiconductor die has a substantially rectangular shape.

38. The semiconductor die as recited in claim 35, wherein the two or more offset planar perimeter surfaces are parallel.

39. The semiconductor die as recited in claim 35, wherein each of the two or more offset planar perimeter surfaces are polished surfaces.

41. (Thrice Amended) A semiconductor die comprising:

a first planar surface;

G5 cont'd

a second planar surface opposite the first planar surface;

one or more perimeter edges transverse to and extending between the first planar surface and the second planar surface; and

G5 and

at least one perimeter edge having two or more offset planar surfaces, where the offset planar surfaces are substantially transverse to the first planar surface or the second planar surface with one of the offset planar surfaces extending from the first planar surface and the other of the offset planar surfaces extending from the second planar surface; and

each offset planar surface having a ground or polished surface.

42. The semiconductor die as recited in claim 41, wherein the semiconductor die comprises a rectangular die.

G6

43. (Amended) The semiconductor die as recited in claim 41, wherein each perimeter edge includes offset planar surfaces that are substantially parallel to one another, each of the offset planar surfaces on each perimeter edge are substantially transverse to the first planar surface and the second planar surface with one of the offset planar surfaces extending from the first planar surface and the other of the offset planar surfaces extending from the second planar surface.